

A cross-sectional view of a semiconductor device. The device consists of a substrate 100 with a series of horizontal layers 103, 104, 105, and 106. These layers are interconnected by vertical conductive paths 113, 115, 116, 117, and 118. The top surface is covered by a layer 127, which has openings or vias 133 leading down to the horizontal layers. A bottom layer 136 is also shown.

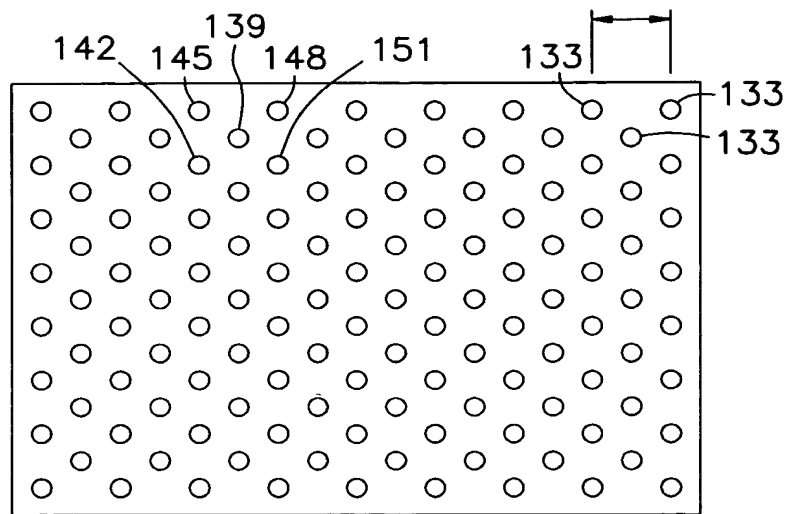


Figure 1B

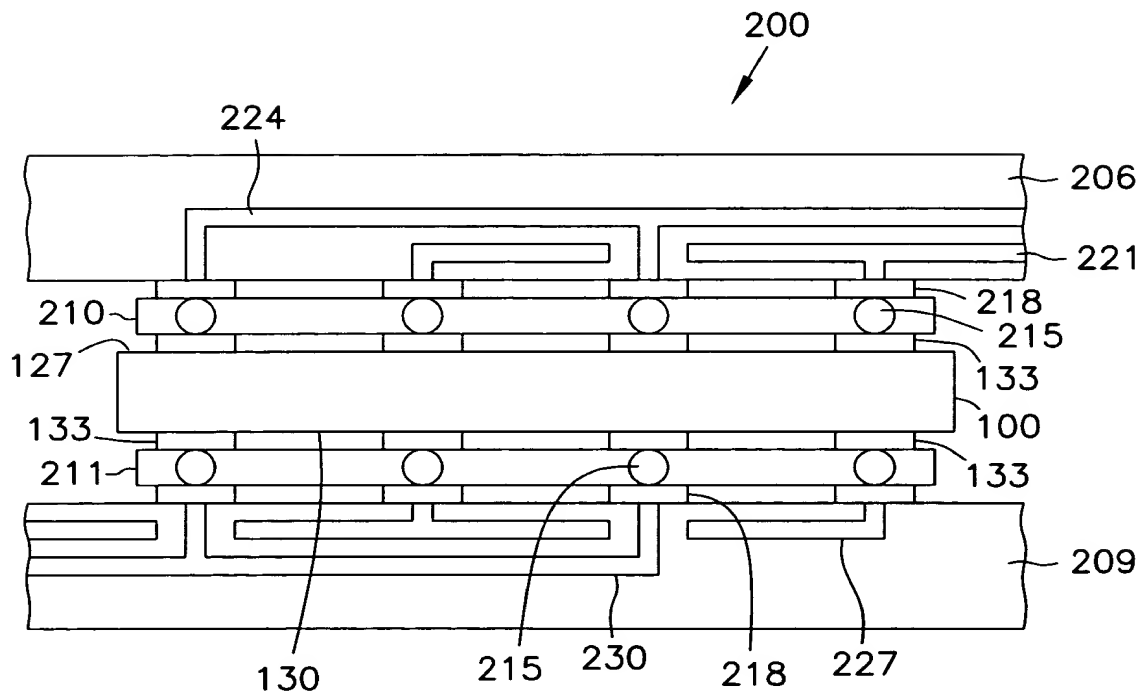


Figure 2



TITLE: HIGH PERFORMANCE CAPACITOR
INVENTOR NAME: Larry E. Mosley
SERIAL NO.: 09/473,315

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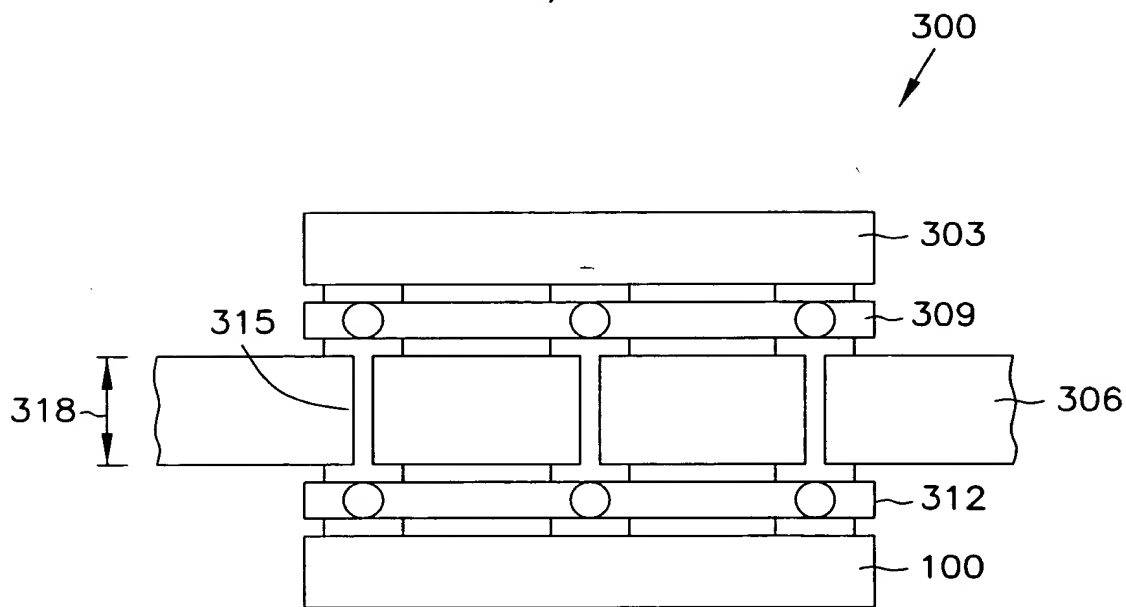


Figure 3

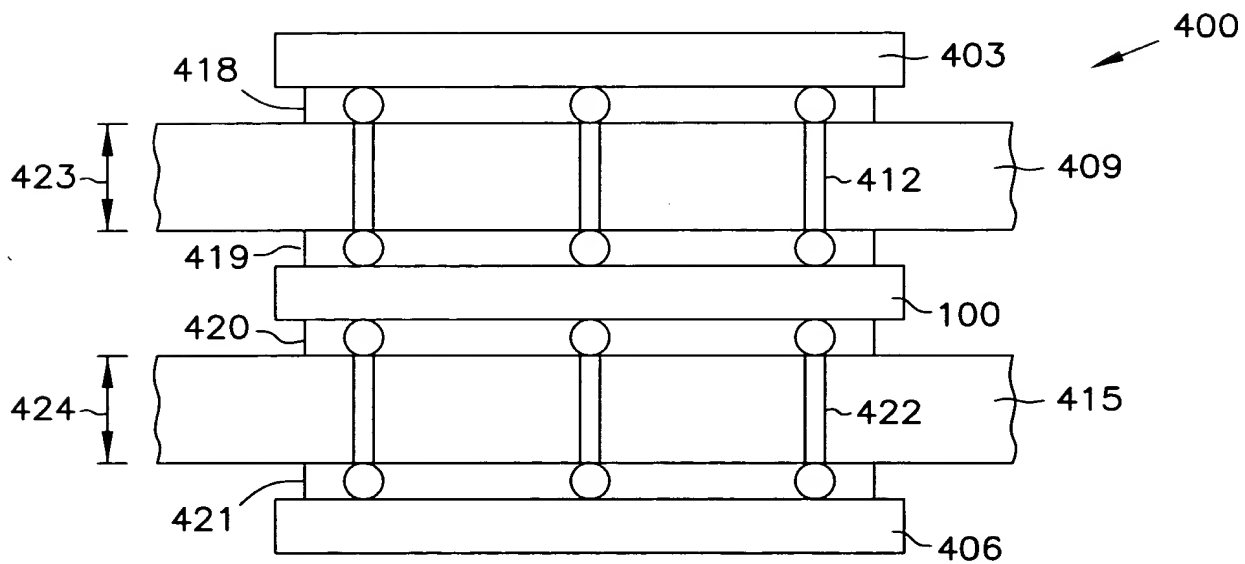


Figure 4



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REPLACEMENT SHEET

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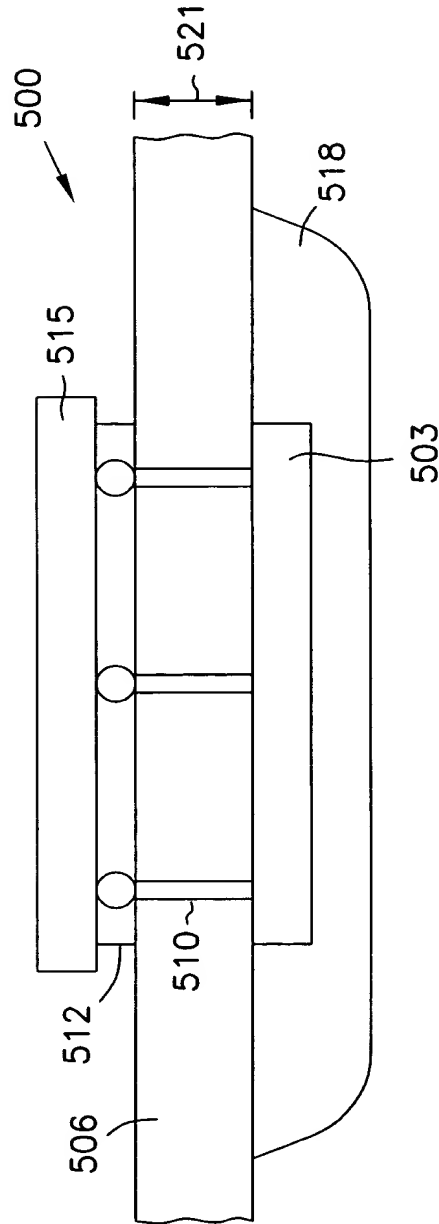


Figure 5